Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-17 are pending in the application, with claims 1, 14, and 16 being the independent claims. Claims 1 and 14-15 are sought to be amended. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 103

Claims 1-17 stand rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over U.S. Pat. No. 5,694,481 to Lam et al. ("Lam") and U.S. Pat. No. 6,285,369 to Kross et al. ("Kross"). Applicants respectfully traverse.

Lam is directed to a method of imaging layers of an integrated circuit (IC), and generating an initial schematic diagram based on the images. Lam neither teaches nor suggests a method or system for editing the initial schematics once they have been produced. The only reference Lam makes to such editing is to say "the resulting graphical schematic database can be edited using the schematic capture tool provided by the EDA vendor." *See*, Lam, col. 17, lines 30-32. The present application on the other hand, is directed to a schematic editor. Since Lam is not directed to a schematic editor and merely states that any other system can be used for editing the schematics produced

by the system of Lam, Applicants respectfully submit that it would not be obvious to one of skill in the art to use Lam as a schematic editor.

Additionally, regarding claim 1, the Examiner stated that the "layer images" of Lam were read to be the same as the "pages" recited in claim 1. Applicants respectfully disagree. As stated above, Lam is directed to a method of producing an initial schematic from a series of images. "Layer images" in Lam refer to images of actual physical layers of the circuit, including the metal and polysilicon layers. In the present application, "pages" refers to a viewable area of the schematic at a given time within the editor. The number of "pages" are not dependent on the layers of silicon, and there are no actual images used in the present invention, only symbolic representations. A schematic having a number of pages refers to the symbolic representation of the integrated circuit (IC) layout, in terms of transistors, logic gates, and other elements. An IC layout can be schematically represented as a hierarchy of functional blocks; alternatively, the IC layout can be represented by flat schematics, which display all the details of the functional blocks and have no hierarchy. In most cases, a symbolic representation of an entire IC or portions of an IC require more than one page to display all the information. Thus, a single layer of the device may, when represented schematically, extend over several pages. Therefore, Lam neither teaches or suggests editing a schematic having a number of pages, as recited in claim 1.

Accordingly, Lam makes no mention of a multi-page schematic or of cutting and pasting a cut portion from one page of the multi-page schematic to another page. Kross is related to general design information and makes no mention of schematics or cutting and pasting portions of a schematic, nor does the Office Action even allege this.

Accordingly, the combination of Lam and Kross neither teaches nor suggests the cutting or pasting modules recited in claim 1.

Further, Lam neither teaches nor suggests a module for connecting nets having the same label located on the same schematic page. As discussed above, Lam does not discuss schematic pages. Lam also does not connect nets based on their labels. Although the Examiner cites Lam, col. 11, lines 12-20, Applicants respectfully submit that this section of Lam does not teach or suggest connecting nets having the same label. In fact, this section states that Lam marks clusters that are initially labeled as being unconnected, which is contrary to the idea of nets having the same label.

Lam discusses a design tool used to produce an initial schematic, but offers no details concerning a system for editing schematics. Lam neither teaches nor suggests, among other things, using schematics having a number of pages or connecting nets having the same label located on the same schematic page, as recited in claim 1. Kross neither teaches nor suggests, among other things, cutting and/or pasting a portion of a schematic from or onto any one of the schematic pages, as further recited in claim 1. Since neither Lam nor Kross, alone or in combination, teach every element of claim 1, Applicants respectfully submit that claim 1 is patentable over the combination of Lam and Kross. Reconsideration and withdrawal of the rejection of claim 1 is respectfully requested.

As claims 2-13 depend either directly or indirectly from claim 1, Applicants respectfully submit that claims 2-13 are patentable over the combination of Lam and Kross for at least the reasons discussed with respect to claim 1. Reconsideration and withdrawal of the rejections of claims 2-13 are respectfully requested.

Additionally, regarding claim 2, the Examiner states that Kross discusses retrieving a design from a database. Applicants respectfully submit that simply retrieving a design from a database is not the same as searching for features within a single design or "searching for objects within the schematic netlist," as recited in claim 2.

Regarding claim 3, the citation from Lam noted by the Examiner describes the labeling of a group of pixels from the images of the physical layers of the integrated circuit. Claim 3, however, is directed to a signal label on a symbolic representation of the integrated circuit. Thus, the label described in Lam is different from the signal label recited in claim 3. Similarly, regarding claim 6, locating the physical location of a standard cell on an image layer, as discussed in Lam, is different from locating the standard cell within a schematic, as recited in claim 6.

Regarding claims 4 and 7, since Lam discusses image layers rather than pages of a schematic, Lam neither teaches nor suggests providing a list of signal labels found on a preselected schematic page, as recited in claim 4, or providing a list of cells found on a preselected schematic page, as recited in claim 7. Further, Lam neither teaches nor suggests an ability to select only portions of the integrated circuit, much less portions of a schematic through a preselected schematic page.

Regarding claim 11, the Examiner states that it would be obvious to make parts of an image invisible so that changed or deleted features do not show up on the completed design. Applicants respectfully submit that claim 11 does not recite rendering labels invisible on changed or deleted features. One purpose of rendering the labels on a particular page invisible is to make the schematics clearer, and the labels can be related to extant features, not only changed or deleted features. Thus, for example, labels that are rendered invisible may be local labels. Further, claim 11 recites rendering invisible

the labels on a current active page or on all the schematic pages. As neither Lam nor Kross discuss pages, Applicants respectfully submit that the combination of Lam and Kross neither teaches nor suggests rendering invisible the labels on a current active page or on all the schematic pages.

Regarding claim 12, the Examiner alleges that adding IN/OUT elements to pin segments is analogous to the function of adding and deleting features in an image editor. However, as discussed in the specification, adding IN/OUT elements to pin segments is performed by a dedicated algorithm and is unique to symbolic representations of integrated circuits. Thus, adding IN/OUT elements to pin segments cannot be compared to regular editing functions such as adding or deleting.

Similarly, regarding claim 13 and as discussed in the specification, cutting a net on a schematic and providing a signal label to the two cut ends of the net are performed by a dedicated algorithm that creates and validates new nets in addition to creating visible text labels for the new nets. Thus, the cutting and providing steps recited in claim 13 cannot be compared to regular editing functions such as adding or deleting.

Regarding claims 14-17, Applicants respectfully submit that claims 14-17 are patentable over the combination of Lam and Kross for at least the same reasons discussed with respect to claim 1. Lam is directed to a software viewer for displaying high magnification images of an IC. The layers of metal and polysilicon are referred to as "layers" in Lam. In the present application, "pages" refers to the schematic pages of a schematic editor. The number of pages used by the editor are unrelated to the number of layers on an IC. Thus, Lam neither teaches nor suggests a project viewer software configured to edit a schematic having a number of pages.

Further, the Examiner interprets "edges" and "edge clusters" from Lam to "signals" and "segments," respectively. Applicants respectfully disagree with this interpretation. Edges and edge clusters refer to features on the high magnification image layers of the IC of Lam. Signals and segments, as recited in claims 14-17, refer to signal names and wire segments on the symbolic representation of the IC. Since they refer to different elements of their respective subjects, Applicants respectfully submit that edges and edge clusters from Lam cannot be read onto the signals and segments of claims 14-17. Kross also does not teach or suggest these features. Reconsideration and withdrawal of the rejection of claims 14-17 are respectfully requested.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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